```
if(R1==0) {R1=R5; R2=R6; R3=R7; R4=R8;}
else      {R1=R9; R2=R10; R3=R11; R4=R12;}
R10 = 0;
```

FIG. 1 PRIOR ART

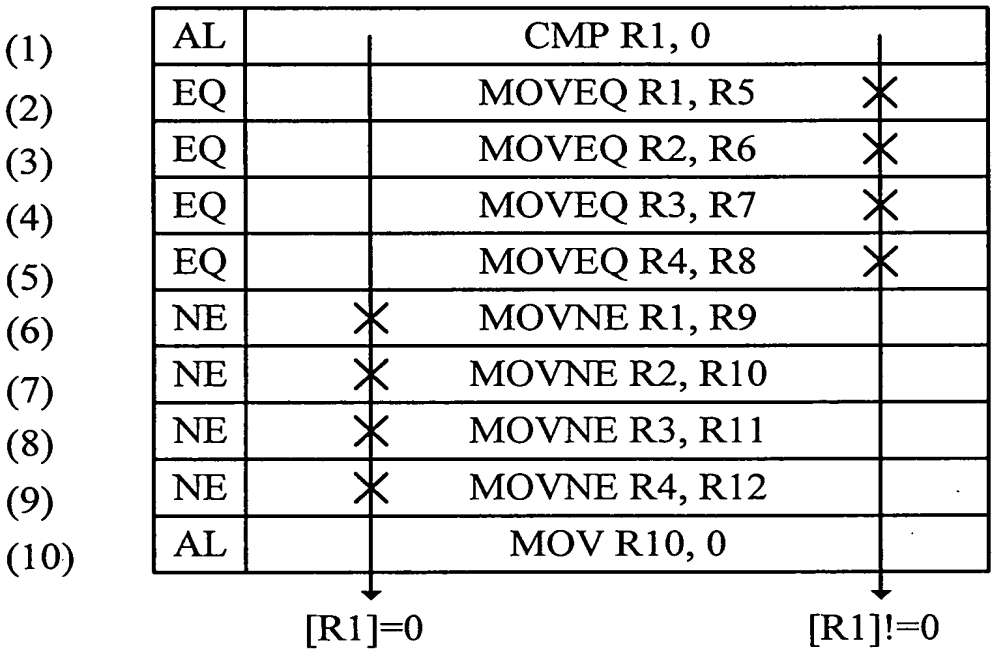


FIG. 2 PRIOR ART

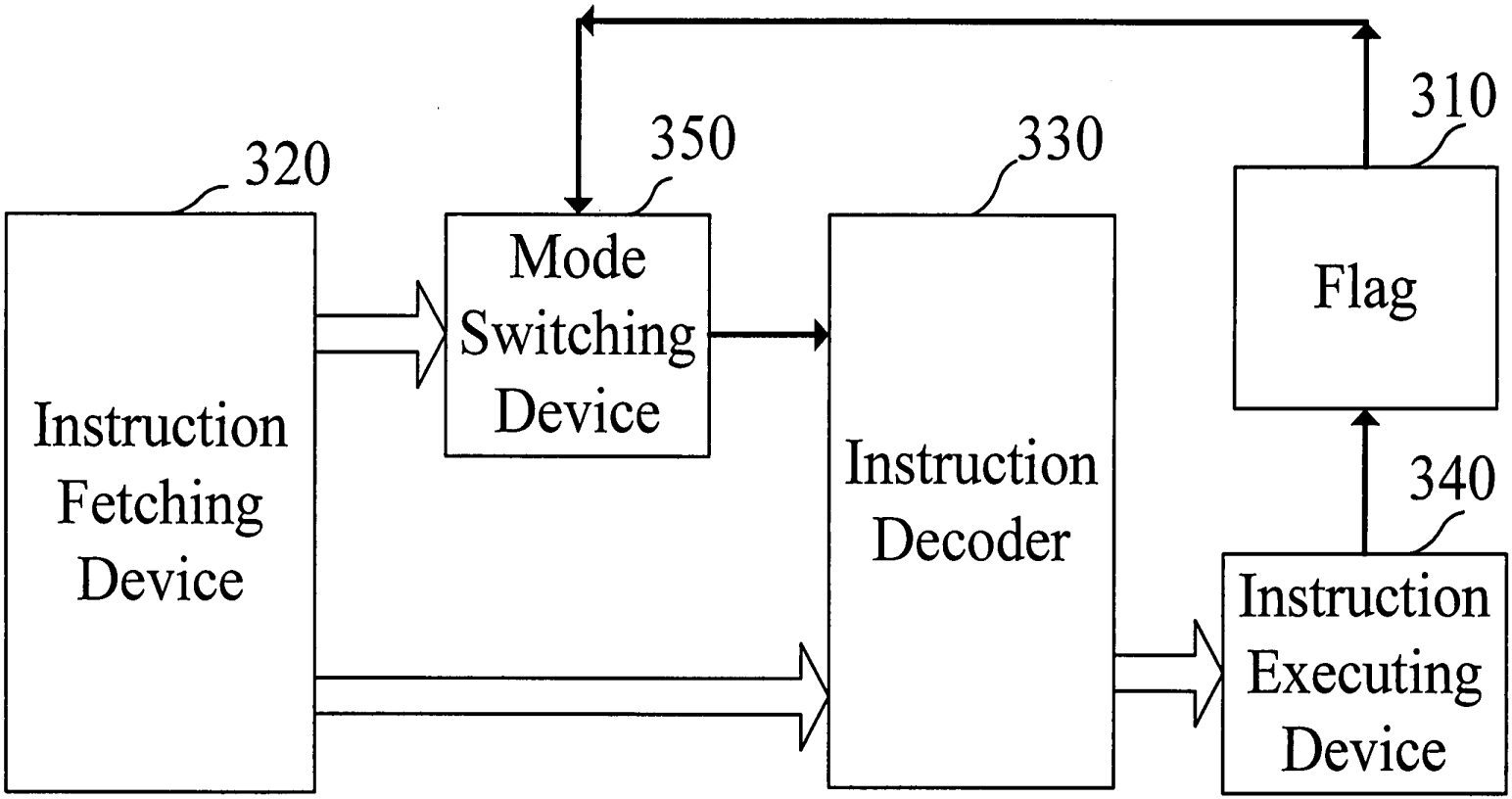
320
350
330
310
Instruction Fetching Device
Mode Switching Device
Instruction Decoder
Flag
340
Instruction Executing Device

FIG. 3

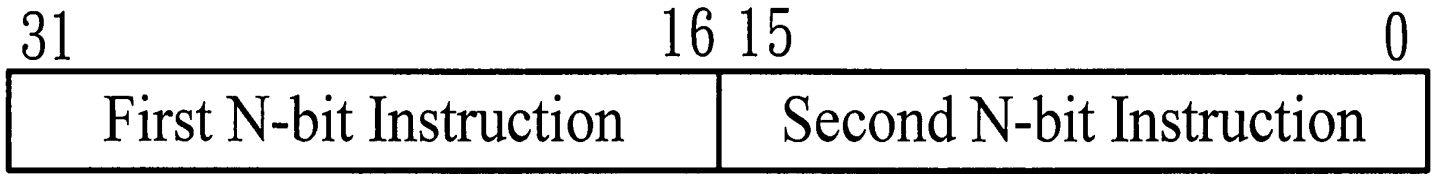
31
16 15
0
First N-bit Instruction
Second N-bit Instruction

FIG. 4

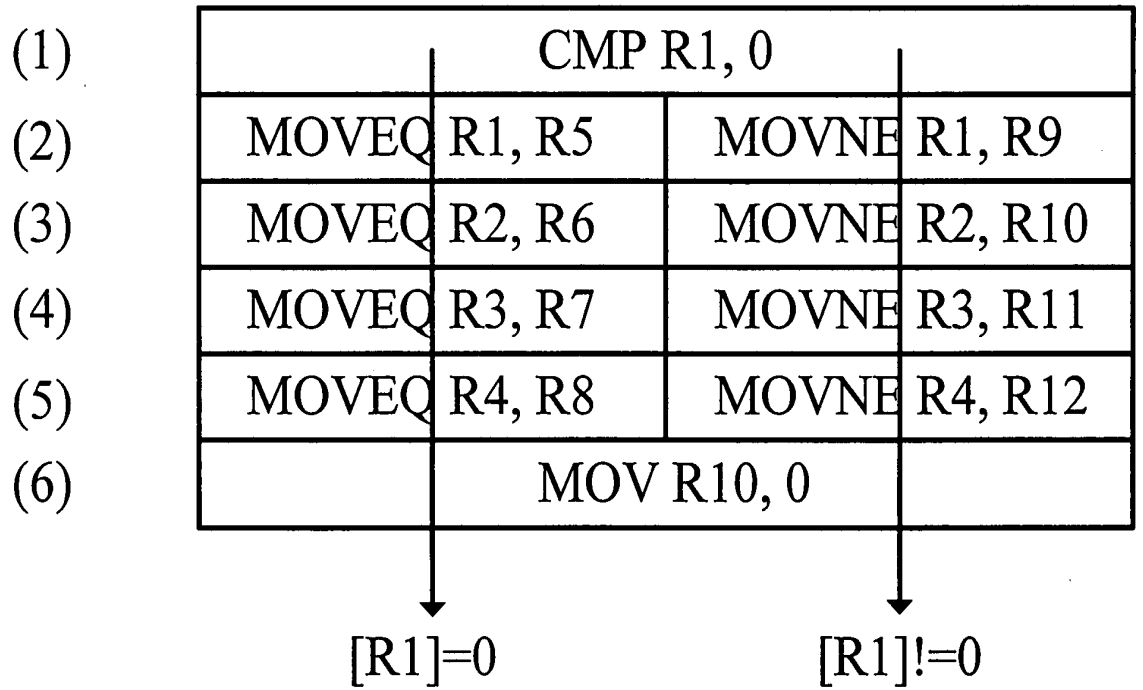
(1)
CMP R1, 0
(2)
MOVEQ R1, R5
MOVNE R1, R9
(3)
MOVEQ R2, R6
MOVNE R2, R10
(4)
MOVEQ R3, R7
MOVNE R3, R11
(5)
MOVEQ R4, R8
MOVNE R4, R12
(6)
MOV R10, 0
[R1]=0
[R1]!=0

FIG. 5

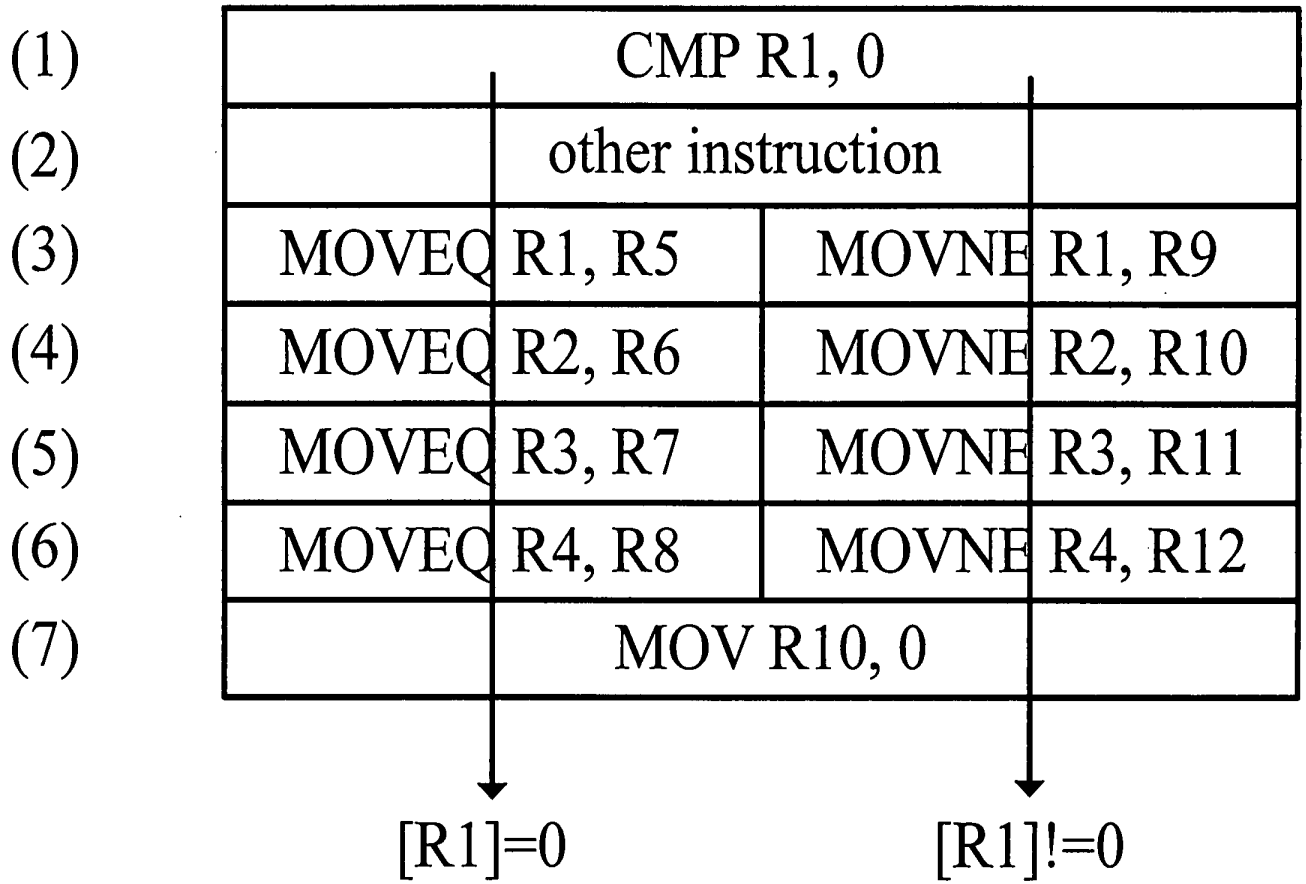
(1)
(2)
(3)
(4)
(5)
(6)
(7)
CMP R1, 0
other instruction
MOVEQ R1, R5
MOVNE R1, R9
MOVEQ R2, R6
MOVNE R2, R10
MOVEQ R3, R7
MOVNE R3, R11
MOVEQ R4, R8
MOVNE R4, R12
MOV R10, 0
[R1]=0
[R1]!=0

FIG. 6

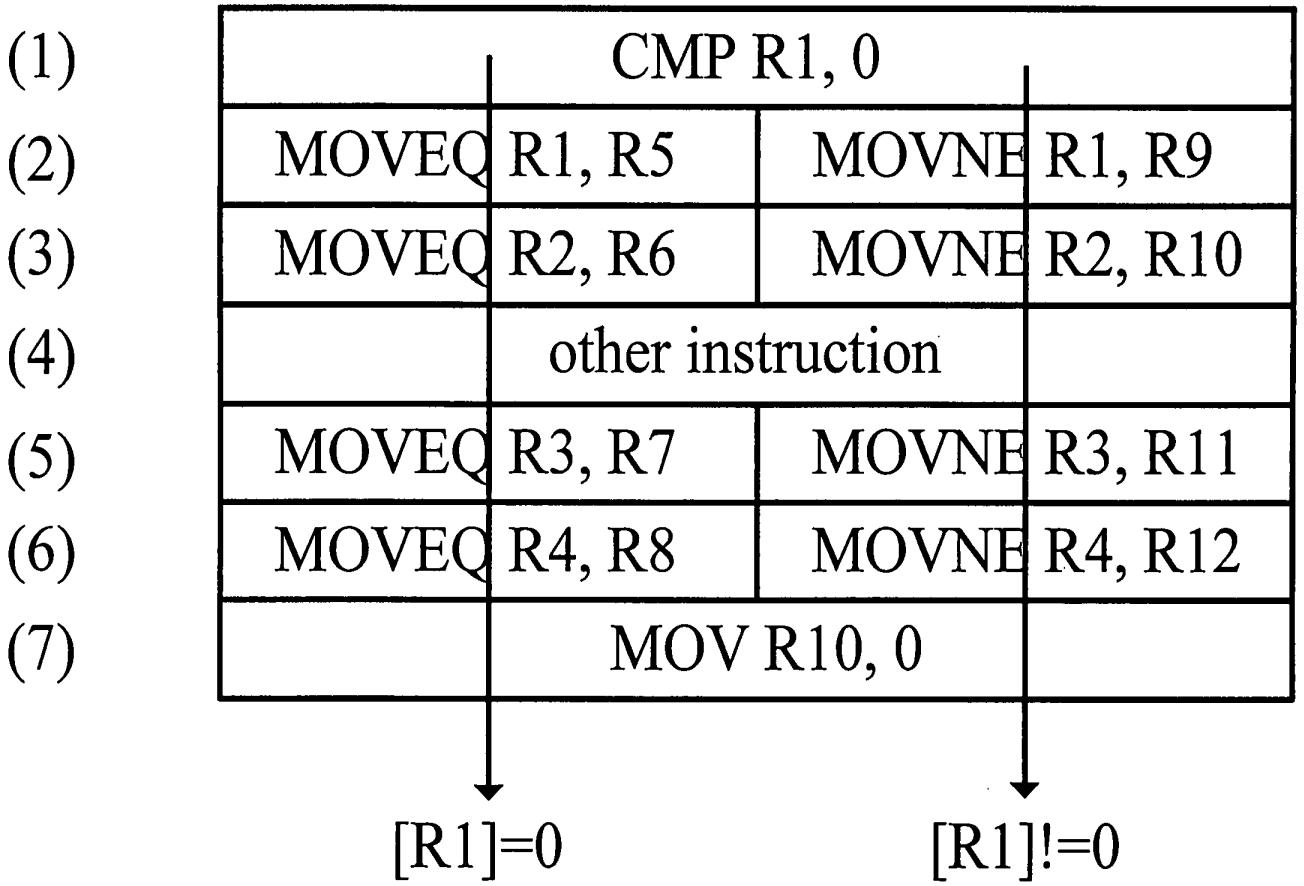
(1)
(2)
(3)
(4)
(5)
(6)
(7)
CMP R1, 0
MOVEQ R1, R5
MOVNE R1, R9
MOVEQ R2, R6
MOVNE R2, R10
other instruction
MOVEQ R3, R7
MOVNE R3, R11
MOVEQ R4, R8
MOVNE R4, R12
MOV R10, 0
[R1]=0
[R1]!=0

FIG. 7

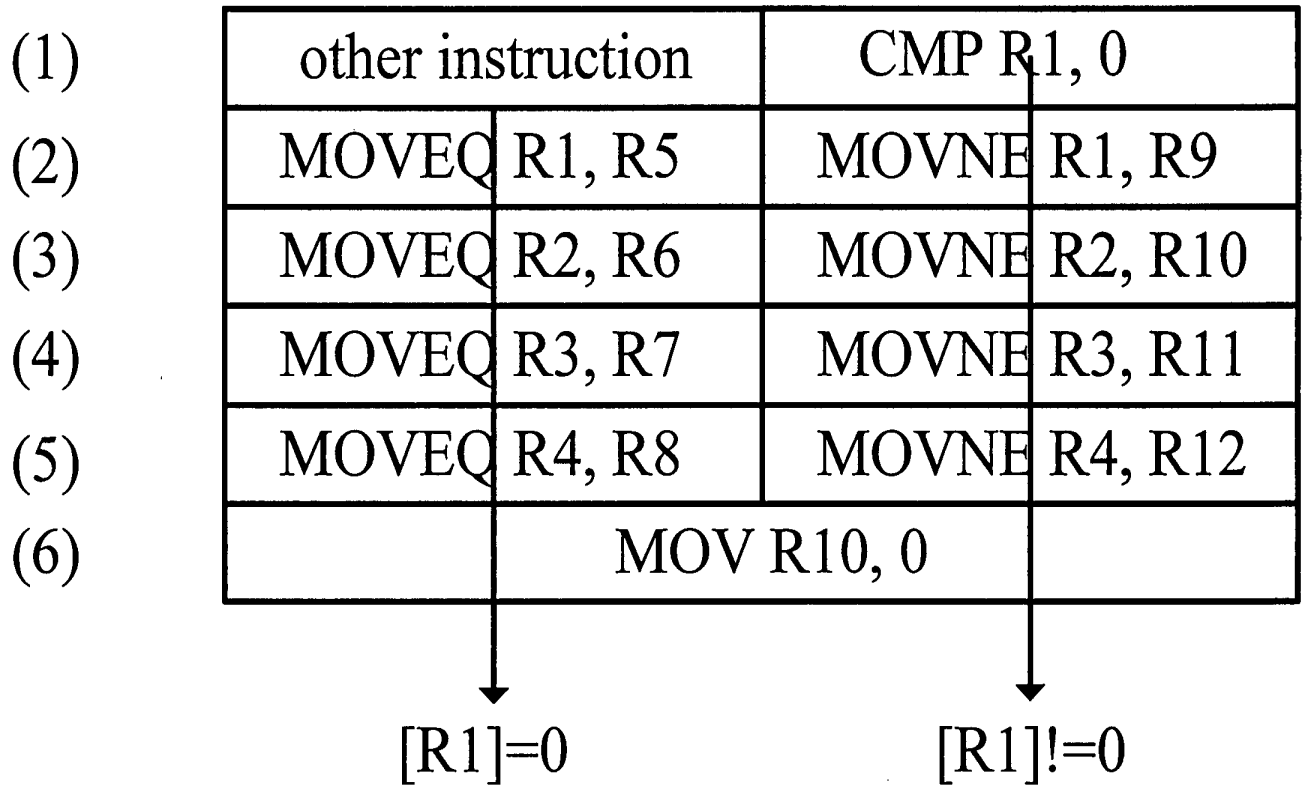
(1)
other instruction
CMP R1, 0
(2)
MOVEQ R1, R5
MOVNE R1, R9
(3)
MOVEQ R2, R6
MOVNE R2, R10
(4)
MOVEQ R3, R7
MOVNE R3, R11
(5)
MOVEQ R4, R8
MOVNE R4, R12
(6)
MOV R10, 0
[R1]=0
[R1]!=0

FIG. 8